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MAR 27 2007

### REMARKS

The present response is intended to be fully responsive to the rejection raised in the Office Action, and is believed to place the application in condition for allowance. Further, the Applicants do not acquiesce to any portion of the Office Action not particularly addressed. Favorable reconsideration and allowance of the application is respectfully requested.

In the Office Action, the Examiner noted that claims 1-50 are pending and are rejected. The Examiner objected to claim 9. In view of the following discussion, the Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

### I. OBJECTIONS

The Examiner objected to claim 9, stating that "it is unclear what is 1<sup>st</sup> trigger input is connected to, as the claim 9, dependent on claim 8, only discloses, '...trigger signal is applied to the second and third trigger inputs....'" (Final Office Action, p. 5). The Examiner further stated that claim 9 leaves the picture incomplete as to what is connected to the "third logic input" of "a third logic". (Final Office Action, p. 5).

The Examiner's objection of claim 9 is clear error. First, the Examiner poses the question of to what the first trigger input is connected. However, claim 9 does not explicitly recite "a first trigger input." The fact that claim 9 recites "the trigger signal is applied to the second and third trigger inputs" is irrelevant to the feature of "the first trigger input." Applicants respectfully request clarification as to why claim 9 is being objected to for a feature it does not explicitly recite.

Claim 9 depends on claim 8, which does recite that "a trigger signal is received at the first trigger input." Applicants are unaware of any law, rule, or otherwise that requires an element in a claim to be "connected to" another element. One skilled in the art will clearly understand a feature of a second logic having a trigger input that receives a trigger signal, as recited in claim 8. As for the "third logic input," Applicants again assert that there is no requirement that an element be "connected to" another element.

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One skilled in the art will clearly understand a feature of a third logic having a third logic input that receives a new value of the first data. Section 112 requires no more. Therefore, Applicants respectfully request that the present objection to claim 9 be withdrawn.

Finally, if the Examiner decides to maintain the present objection, Applicants respectfully request that the present objection be a "rejection" under 35 U.S.C. §112, second paragraph for purposes of Appeal. The Examiner's argument that claim 9 is "unclear" is in essence stating that claim 9 is indefinite, which should be a rejection rather than an objection. Should the Examiner continue to assert that claim 9 is unclear for the reasons given, as well as continue to assert the rejections discussed below, Applicants may desire to argue clarity of claim 9 before the Board of Appeal.

## **II. REJECTION OF CLAIMS UNDER 35 U.S.C. §103**

### **A. Claims 1-6, 19-36, 38 and 44-46**

The Examiner rejected claims 1-6, 19-36, 38, and 44-46 as being unpatentable over Bhandari et al. (U.S. Patent No. 5,663,900, Issued September 2, 1997) ("BH '900") in view of Klein (U.S. Patent No. 5,771,370, issued June 23, 1998). The Applicants respectfully traverse this rejection.

In the Final Office Action, the Examiner maintains that Bhandari teaches that the second information comprises at least one internal state of the hardware model despite lack of any explicit disclosure, since such information would be vital to any hardware-software co-simulation system. (Final Office Action, p. 3). The Examiner cited U.S. Patent 6,052,524 and U.S. Patent 5,546,562 as showing that "[i]t is well known in the art that co-simulation of hardware and software share information, otherwise it would not be called co-simulation." Applicants agree with the Examiner that co-simulation generally involves sharing of information between hardware and software. However, Applicants do not claim a general exchange of information between hardware and software. Rather, Applicants recite that the second information comprises at least one internal state of the hardware model. In essence, Applicants claim a shared memory for storing first information of a software model and the second information, which allows the software model to directly access at least one internal state of the hardware model. The

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mere fact that co-simulation generally involves sharing information between hardware and software does not teach, suggest, or otherwise render obvious the more specific feature of a shared memory configured to store both information of the software model and internal state information of the hardware model, recited in Applicants' claims. Moreover, as detailed in Applicants' response to the previous Office Action, neither U.S. Patent 6,052,524 nor U.S. Patent 5,546,562 teach or suggest such a feature. Again, Applicants traverse the Examiner's Official Notice and respectfully request that the Examiner provide a reference or references that provide evidence that a shared memory configured to store both software model information and at least one internal state of the hardware model is well known in the art.

The Examiner also maintained that Klein teaches a shared memory for holding first information of a software model and second information of a hardware model, where the software model is capable of directly accessing the second information of the hardware model. (Final Office Action, pp. 8-9). The Examiner stated that "[it] is unclear how [a] 'single coherent view of memory' is patentably different than 'physical shared memory.'" (Final Office Action, p. 4). Performing a simulation with a "view" of memory is an abstract concept. A single coherent view of the memory is not a literal concept, i.e., Klein does not mean that one looks at memory in the ocular sense. The view of memory in Klein is not something tangible that can be held in one's hands. Rather, the single coherent view of memory in Klein refers to software simulation that accounts for all memory in the design being simulated. (Klein, col. 4, lines 15-21). A physical memory, however, is something tangible and is not abstract. A logical software construct does not teach or suggest a physical memory.

The Examiner also stated that Applicants' claims do not recite a physical shared memory. (Office Action, p. 4). Applicants contend that to interpret the claims otherwise is unreasonable. An Applicant is not required to preface each element in an apparatus claim with the term "physical." Claims are read by those skilled in the art in light of the specification. Applicants' claim 1 recites a computing system, an internal bus, reconfigurable hardware logic, control logic, and a shared memory. The shared memory in Applicants' claims is clearly a physical memory and not an abstract concept of memory.

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The Examiner also stated that Applicants' claim a computer system and it is well known in the art that memory present in a computer system is shared by various applications and peripherals. (Final Office Action, p. 4). Applicants do not disagree. However, the general teaching of memory in a computer shared among peripherals and applications does not teach, suggest, or otherwise render obvious the specific feature of a shared memory configured to store first information of a software model and at least one internal state of a hardware model generated in reconfigurable hardware logic, as recited in Applicants' claims 1. The Examiner must analyze the claims as a whole, including all of the features recited therein. Applicants' claims are much more specific than a computer having a shared memory.

As Applicants discussed in response to the previous Office Action, Klein discloses co-simulation of a hardware-software system design using entirely software-based simulators. (See Klein, col. 5, lines 6-65; FIG. 2). Both the logic simulator and the ISS are software-based simulators. The software described in Klein performs the hardware and software simulations with a single coherent view of the memory of the hardware-software system being co-simulated. (Klein, col. 4, lines 15-21). Clearly, the memory referred to in Klein is memory that is part of the design being co-simulated. The Examiner cite to FIG. 1 of Klein actually confirms this teaching. (Final Office Action, p. 5). FIG. 1 of Klein recites "memory of hardware-software system being co-simulated." The plain meaning of that statement is that the memory is part of the hardware-software system, and that such hardware-software system is being co-simulated. There is no contrary meaning in Klein.

The Examiner further noted that Applicants' claims do not make the distinction between memory in a co-simulation system and memory of a design being co-simulated. (Final Office Action, p. 5). Such an interpretation of Applicants' claims is unreasonable. Applicants clearly claim a system for co-simulating a design. In claim 1, the system includes a computing system, an internal bus, a reconfigurable hardware logic, a control logic, and a shared memory. No permissible interpretation of Applicants' claim 1, as understood by one skilled in the art, renders the shared memory part of the design being co-simulated. The shared memory in Applicants' claims is not part of the software model or the hardware model. Rather, the electronic design automation

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system comprises the shared memory.

Finally, Applicants' reference to the fact that Klein teaches a complete software simulation system that does not employ an emulator or other type of reconfigurable hardware was merely meant to point out the differences between Klein and BH'900. BH'900 teaches a system that models a portion of the design in hardware, and another portion of the design in software. Klein, however, does not model any portion of the design in hardware and thus describes a different system. Thus, Klein does not teach or suggest any hardware component (i.e., a shared memory) that can be used in the hardware portion of BH'900 to emulate a portion of a design. Accordingly, Klein does not bridge the substantial gap between Bhandari and Applicants' invention recited in claim 1. Namely, Klein does not provide a teaching or suggestion of a shared memory as recited in Applicants' claim 1 that can be incorporated into or otherwise modify the system of Bhandari to arrive at the invention of Applicants' claim 1. Therefore, Applicants contend that no conceivable combination of Bhandari and Klein renders obvious Applicants' invention of claim 1.

Independent claims 19, 24, 30, 33, 38, and 44 each recite features similar to those of claim 1 emphasized above. For the same reasons discussed above, Applicants contend that no conceivable combination of Bhandari and Klein renders obvious Applicants' invention of claims 19, 24, 30, 33, 38, and 44. Claims 2-6, 20-23, 25-29, 31-32, 34-36, and 45-46 depend from claims 1, 19, 24, 30, 33, 38, and 44 and recite additional features therefor. Since the cited combination does not render obvious Applicants' invention recited in claims 1, 19, 24, 30, 33, 38, and 44, claims 2-6, 20-23, 25-29, 31-32, 34-36, and 45-46 are also nonobvious. Accordingly, Applicants contend that claims 1-6, 19-36, 38, and 44-46 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

#### **B. Claims 7 and 10**

The Examiner rejected claims 7 and 10 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein and further in view of RO'1998. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari

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and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in combination do not render dependent claims 7 and 10 obvious, at least for their dependency upon independent claim 1 (see above). The addition of RO'1998 does not correct the shortcomings of Bhandari and/or Klein.

For example, RO'1988 teaches Q-modules without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or RO'1998 do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claim 1. Therefore, dependent claims 7 and 10, which depend either directly or indirectly from claim 1, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

### **C. Claims 8-9 and 11-18**

The Examiner rejected claims 8-9 and 11-18 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of RO'1998, further in view of VA'1997. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, Klein, and of RO'1998 into the instant section. Applicants submit that Bhandari, Klein, and/or RO'1998, alone or in combination, do not render obvious dependent claims 8, 9, and 11-18, at least for their dependency upon independent claim 1 (see above). The addition of VA'1997 does not correct the shortcomings of Bhandari, Klein, and/or RO'1998.

For example, VA'1997 teaches delay insensitive modules without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, RO'1998, and/or VA'1997, do not teach or suggest these features, no

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conceivable combination of these references can teach or suggest Applicants' invention of claim 1. Therefore, dependent claims 8, 9, and 11-18, which depend either directly or indirectly from claim 1, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

#### **D. Claim 37**

The Examiner rejected claim 37 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, and further in view of Butts. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in combination do not render obvious dependent claim 37, at least for its dependency upon independent claim 33 (see above). The addition of Butts does not correct the shortcomings of Bhandari and/or Klein.

Butts teaches interconnected FPGAs without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or Butts, do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claim 33. Therefore, dependent claim 37, which depends from claim 33, is nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of claim 37 be withdrawn.

#### **E. Claims 39-43 and 47-50**

The Examiner rejected claims 39-43 and 47-50 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of BI'1997. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in

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combination do not render obvious dependent claims 39-43 and 47-50, at least for their dependency upon independent claims 38 and 44 (see above). The addition of BI'1997 does not correct the shortcomings of Bhandari and/or Klein.

BI'1997 teaches hardware/software co-simulation without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or BI'1997, do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claims 38 and 44. Therefore, dependent claims 39-43 and 47-50, which depend from claims 38 and 44, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

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**CONCLUSION**

In view of the foregoing, the Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

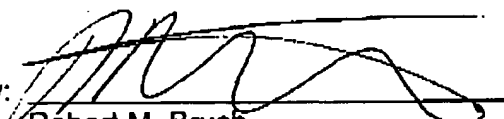
If, however, the Office believes that any unresolved issues still exist or if, in the opinion of the Office, a telephone conference would expedite passing the present application to issue, the Office is invited to call the undersigned attorney directly at 732-917-6320 or the office of the undersigned attorney at 732-978-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

Moser IP Law Group

Date: March 27, 2007

By:

  
Robert M. Brush  
Registration No. 45,710

MOSER IP LAW GROUP  
1040 Broad Street – 2<sup>nd</sup> Floor  
Shrewsbury, NJ 07702  
(732) 935-7100

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